



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jri Lee et al. Examiner: Not yet assigned  
Serial No.: 10/616,021 Group Art Unit: 2816  
Filed: July 9, 2003 Docket: G&C 30448.116-US-U1  
Title: 40-GB/S CLOCK AND DATA RECOVERY CIRCUIT IN 0.18 UM TECHNOLOGY

**CERTIFICATE OF MAILING OR TRANSMISSION UNDER 37 CFR 1.8**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 22, 2003.

By:   
Name: George H. Gates

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

We are transmitting herewith the attached:

- Transmittal sheet, in duplicate, containing a Certificate of Mailing under 37 CFR 1.8.
- Information Disclosure Statement and Form PTO-1449.
- Cited Reference(s).
- Return postcard.

Please consider this a **PETITION FOR EXTENSION OF TIME** for a sufficient number of months to enter these papers, if appropriate.

Please charge all fees to Deposit Account No. 50-0494 of Gates & Cooper LLP. A duplicate of this paper is enclosed.

CUSTOMER NUMBER 22462  
GATES & COOPER LLP  
Howard Hughes Center  
6701 Center Drive West, Suite 1050  
Los Angeles, CA 90045  
(310) 641-8797

By:   
Name: George H. Gates  
Reg. No.: 33,500  
GHG/sjm

(PTO TRANSMITTAL - GENERAL)

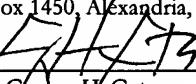
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OCT 27 2003  
PATENT & TRADEMARK OFFICE

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**INFORMATION DISCLOSURE STATEMENT (37 C.F.R. §1.97(b))**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

With regard to the above-identified application, the items of information listed on the enclosed Form 1449 are brought to the attention of the Examiner.

This statement should be considered because it is submitted before the mailing date of a first Office Action on-the-merits. Accordingly, no fee is due for consideration of the items listed on the enclosed Form 1449.

In accordance with 37 C.F.R. §1.98(a)(2), a copy of each document or other information listed on the enclosed Form 1449 is provided.

No representation is made that a reference is "prior art" within the meaning of 35 U.S.C. §§ 102 and 103 and Applicants reserve the right, pursuant to 37 C.F.R. § 1.131 or otherwise, to establish that the reference(s) are not "prior art". Moreover, Applicants do not represent that a reference has been thoroughly reviewed or that any relevance of any portion of a reference is intended.

Consideration of the items listed is respectfully requested. Pursuant to the provisions of M.P.E.P. 609, it is requested that the Examiner return a copy of the attached Form 1449, marked as being considered and initialed by the Examiner, to the undersigned with the next official communication.

Please direct any response or inquiry to the below-signed attorney at (310) 641-8797.

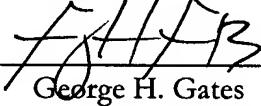
Respectfully submitted,

GATES & COOPER LLP  
Attorneys for Applicant(s)

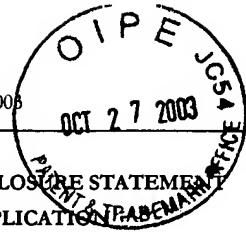
Howard Hughes Center  
6701 Center Drive West, Suite 1050  
Los Angeles, California 90045  
(310) 641-8797

Date: October 22, 2003

GHG/sjm

By: 

George H. Gates  
Reg. No.: 33,500



Form 1449\*

INFORMATION DISCLOSURE STATEMENT  
IN AN APPLICATION

Docket Number: G&amp;C 30448.116-US-U1

Application Number: 10/616,021

Applicants: Jri Lee et al.

Filing Date: July 9, 2003

Group Art Unit: 2916

U.S. PATENT DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
FOREIGN PATENTS						
	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
						YES
						NO
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)						
	M. Wurzer et al, "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz $f_T$ Silicon Bipolar Technology," IEEE Journal of Solid-State Circuits, Sept. 1999, 34:1320-1324					
	M. Reinhold et al, "A Fully Integrated 40-Gb/s Clock and Data Recovery IC with 1:4 DEMUX in SiGe technology," IEEE Journal of Solid-State Circuits, Dec. 2001, 36:1937-1945					
	J. Cao et al, "OC-192 Receiver in Standard 0.18 $\mu$ m CMOS," ISSCC Dig. Tech. Papers, Feb. 2002, pp. 250-251					
	J. Kim and B. Kim, "A Low Phase-Noise CMOS LC Oscillator with a Ring Structure," ISSCC Dig. of Tech. Papers, Feb. 2000, pp. 430-431					
	T. P. Liu, "A 6.5-GHz Monolithic CMOS Voltage-Controlled Oscillator," ISSCC Dig. of Tech. Papers, Feb. 1999, pp. 404-405					
	J. E. Rogers and J. R. Long, "A 10-Gb/s CDR/DEMUX with LC Delay Line VCO in 0.18 $\mu$ m CMOS," ISSCC Dig. of Tech. Papers, Feb. 2002, pp. 254-255					
	J. Savoj and B. Razavi, "A 10-Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection," ISSCC Dig. Tech. Papers, Feb. 2001, pp. 78-79					
	M. Danesh et al, "A Q-Factor Enhancement Technique for MMIC Inductors," Proc. IEEE Radio Frequency Integrated Circuits Symp., April 1998, pp. 217-220					
	A. Hajimiri and T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," IEEE Journal of Solid-State Circuits, Feb. 1998, pp. 179-194					
	J. D. H. Alexander, "Clock Recovery from Random Binary Data," Electronics Letters, Oct. 1975, 11:541-542					
	B. Razavi et al, "Design Techniques for Low-Voltage High-Speed Digital Bipolar Circuits," IEEE Journal of Solid-State Circuits, March 1994, pp. 332-9					

EXAMINER:	DATE CONSIDERED:
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form for next communication to the Applicant.	